Remarks

Claims 38 – 112 are pending. Independent claims 38, 43, 49, 54, 57, 61, 66, 70, 74, 77, 82, 86, 89, 95, 101 and 107 are amended. The following comments are provided in response to the Examiner's rejections of the claims in light of Toy under § 102 in ¶7 of the Office Action.

Initially, Applicant notes that there seems to be some confusion about what kind of address translation is shown in Toy (U.S. Patent No. 4,400,774). The thrust of the Toy teachings, in fact, are only concerned with data access from a cache *subsequent* to an actual virtual-to-physical translation. There is very little detail, if any, on the actual operation of the address translation buffer.

Apparently, however, there is a perception by the Examiner that this reference depicts a virtual-linear-physical address system, and on this basis the Examiner believes there is "inherently" a linear address generated. *See e.g.*, Office Action, page 3, line 9. This is incorrect, nonetheless, and this can be seen quite plainly from the discussion that follows.

Because the Examiner's rejection based on this reference appears to be based on a faulty assumption, and because there is no prior art known to Applicant that describes or suggests the limitations of the pending claims, Applicant submits that the claims are in condition for allowance.

To begin with, Toy is typical of prior art systems where segmentation and paging are *integrated*, and hence transformation from virtual to physical addresses is performed in one step; *i.e.*, there are no separate segmentation/paging operations during an address translation. This can be verified from the fact that the virtual address in Toy is specifically noted as having a format of the type [segment:page:word]. Toy specifically indicates that the word address bits *are not even translated. See e.g.*, c.3 64 - 69. From this fact alone it can be seen that it is not a true separated segmentation/paging system as in the present invention, *and thus there never is any "linear" address of any kind.*

One of the objects of the present invention as disclosed in the specification on page 4 at lines 22-26, is to achieve the speed and performance advantages of *integral* segmentation and paging, and at the same time, to provide the space compaction and compatibility advantages of *separate* segmentation and paging. Integral segmentation and paging systems such as Toy cannot provide this capability, and do not suggest to - let alone instruct - one of skill in the art how to do so. Moreover, such systems have a number of drawbacks, including the fact that the segments must start on page boundaries, and must be comprised of an integral number of pages, regardless of size.

The present invention is used in environments that have virtual addresses composed of a segment identifier and a segment offset; for a normally calculated physical address, these virtual

addresses must be converted by a segmentation process into a linear address. During the virtual-to-linear translation, the segment offset portion (the lower portion of the virtual address) contributes to both the page and word (or byte) offset of the linear address. This is characteristic of the two step (virtual-to-linear, then linear-to-real) independent segmentation and paging scheme of the environments where the present invention is used. Thus, there is no such separate segmentation process or apparatus disclosed or taught by Toy, because there is no such linear address.

Accordingly, Toy is quite easily distinguishable from the present claims because it does not teach or disclose: (1) a virtual address of the [segment identifier: segment offset] variety; or (2) a linear address of the type used in the present invention; or (3) a virtual-linear address conversion operation. Again, applicant believes the claims already differentiate from such a system, but have further amended the claims to better clarify the scope of the present invention. As the Examiner can verify, the new amendments track these distinctions fairly closely. To further distinguish claims 81 – 112, they have been amended to indicate that, unlike Toy, all of the virtual address is translated when a calculated linear address is required.

In brief, Applicant was the first to conceive and describe a viable mechanism that provides fast memory references in computer systems that use independent segmentation plus optional paging for address translations. This type of speculative operation allows for faster program execution, because data at a particular physical memory location can be retrieved faster than with conventional prior art memory access schemes. There is simply no teaching, suggestion or hint in Toy (or elsewhere) on how to achieve such functionality in the kind of environment where the applicant's invention is used. Accordingly, applicants submit that the claims should be in condition for allowance.

Should the Examiner believe it that it would be helpful to discuss any of the above points in person, Applicant is open to a telephone conference (408-342-1862) at any convenient time.

Respectfully submitted,

Date: July 30, 1999

J. Nicholas Gross, Attorney, Reg. No. 34,175

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 30th day of July 1999.